COMPLEMENTARY TRANSISTORS HAVING DIFFERENT SOURCE AND DRAIN EXTENSION SPACING CONTROLLED BY DIFFERENT SPACER SIZES

ABSTRACT

Disclosed is a method of forming an integrated circuit structure having first-type transistors, such as P-type field effect transistors (PFETs) and complementary second-type transistors, such as N-type field effect transistors (NFETs) on the same substrate. More specifically, the invention forms gate conductors above channel regions in the substrate, sidewall spacers adjacent the gate conductors, and source and drain extensions in the substrate. The sidewall spacers are larger (extend further from the gate conductor) in the PFETs than in the NFETs. The sidewall spacers align the source and drain extensions during the implanting process. Therefore, the larger sidewall spacers position (align) the source and drain implants further from the channel region for the PFETs when compared to the NFETs. Then, during the subsequent annealing processes, the faster moving PFET impurities will be restrained from diffusing too far into the channel region under the gate conductor. This prevents the short channel effect that occurs when the source and drain impurities extend too far beneath the gate conductor and short out the channel region.